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Cong (Callie) Hao

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RESEARCH AREA

- **High-performance reconfigurable computing**: FPGA, computer architecture
- **Machine learning and system**: ML algorithm/system co-design, graph neural network (GNN)
- **Electronic design automation (EDA)**: high-level synthesis (HLS), ML-assisted EDA, physical design

PROFESSIONAL APPOINTMENTS

2022.01 - present	**Assistant Professor**	School of Electrical and Computer Engineering Georgia Institute of Technology, USA
2020.09 - 2021.12	**Faculty Fellow** **transitional position due to Visa delay*	School of Electrical and Computer Engineering Georgia Institute of Technology, USA
2017.12 - 2020.09	**Postdoctoral Researcher**	School of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, USA

EDUCATION

Ph.D.	Electrical Engineering	Waseda University, Japan	2014 - 2017
M.S.	Electrical Engineering	Waseda University, Japan	2010 - 2012
M.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2011 - 2014
B.S.	Computer Science & Engineering	Shanghai Jiao Tong University, China	2007 - 2011

HONORS AND AWARDS

• International, National, and Best Paper Awards

2024	**NSF CAREER Award**, National Science Foundation, CISE, SHF
2023	**The Intel Rising Star Faculty Award (RSA)**, Intel
2023	**FPL Community Award** (for major open-source contributions), FPL
2023	**Best Paper Award**, IEEE Design Automation Conference (DAC)
2023	**Best Paper Runner-up**, IEEE FCCM
2022	**Amazon Research Award** (in AWS credit)
2022	**Best Paper Nomination**, IEEE ASAP
2022	**Sony Faculty Innovation Award**, Sony Group Corp. (declined)
2022	**Sutterfield Family Early Career Professorship**, Georgia Tech
2021	**Best Paper Award**, ACM Great Lakes Symposium on VLSI (GLSVLSI)
2020	**Third place winner**, IEEE Design Automation Conference (DAC) System Design Contest
2019	**First place winner** (FPGA track, 1/58), IEEE DAC System Design Contest
	First place winner (GPU track, 1/52), IEEE DAC System Design Contest
2019	**Best Poster Award**, ICML Workshop
2018	**Student Innovation Award**, IEEE HPEC Graph Challenge
2018	**Third place winner** (FPGA track, 3/62), IEEE DAC System Design Contest
2018	**Distinguished Project Award**, Boeing Global Technology
2016	**Best Student Paper**, IEEE International New Circuits and Systems Conference
2015	**Best Student Paper**, IEEE International Conference on ASIC
2015	**Young Student Fellow Award**, IEEE Design Automation Conference
2015	**Excellent Paper Award**, ISIPS, Graduate School of IPS, Japan

2013 **Best Student Paper**, IEEE International Conference on ASIC
2013 **Google Anita Borg Memorial Scholarship** (1.5K US$)
2013 **IEICE VLD Excellent Student Award**, IEEE Asia and South Pacific Design Automation Conference
2012 **Best Paper Nomination**, International Symposium on VLSI Design, Automation and Test

• Institute and School Awards

2024 **CIOS (Course Instruction Opinion Survey) Honor Roll**, Georgia Tech
2023 **Student Recognition of Excellence in Teaching**, Georgia Tech
2022 **Student Recognition of Excellence in Teaching**, Georgia Tech

• Student Awards

2022 **Qualcomm Innovation Fellowship Finalist**, Qualcomm, Stefan Abi-Karam, Dejia Xu
2023 **CRNCH PhD Fellowship**, Georgia Tech ECE, Lakshmi Sathidevi
2022 **SIGDA University Demonstration third place**, IEEE DAC, Rishov Sarkar
2022 **CRNCH PhD Fellowship**, Georgia Tech ECE, Rishov Sarkar
2022 **Qualcomm Innovation Fellowship**, Qualcomm, Rishov Sarkar, Zhiwen Fan

RESEARCH FUNDING

My share total amount: $2,876,810 (2.8M)

• As Principal Investigator

NSF **Title: CAREER: Next Generation of High-Level Synthesis for Agile Architectural Design (ArchHLS)**
Division of Computing and Communication Foundations (CCF)
Role: Single PI
Year: 2024 - 2029. Total = $560,000; My share = $560,000.

NSF **Title: CSR: Small: Multi-FPGA System for Real-time Fraud Detection with Large-scale Dynamic Graphs**
Division of Computer and Network Systems (CNS)
Role: Single PI
Year: 2024 - 2026. Total = $554,699; My share = $554,699.

Intel **Unrestricted gift**
Intel Rising Star Award 2023
Role: Single PI
Year: 2024 - *. Total = $50,000; My share = $50,000.

DoE **Title: Intelligent Experiments Through Real-time AI: Fast Data Processing and Autonomous Detector Control for sPHENIX and Future EIC Detectors**
Role: Institute PI (Lead-PI: Ming Xiong Liu, Co-PIs: Nhan Tran, Gunther M Roland, Dantong Yu, Joachim Schambach)
Year: 2023 - 2025. Total = $2,000,000; My share = $128,000.

Samsung **Title: Killing Data before Training: Smart Sampling, Filtering, and Compressing in Smart SSD for Data and Communication Reduction**
Role: Single PI
Year: 2023 - 2024. Total = $75,000.

CISCO **Title: Implicit Neural Representation on Hardware: a New Path to Three Orders of Memory and Computation Reduction**
Role: Single PI
Year: 2023 - 2024. Total = $100,000.

NSF **Title: Collaborative Research: Small: Machine Learning-assisted Modeling and Design of Approximate Computing with Generalizability and Interpretability**
Directorate for Engineering (ENG)
Role: Institute PI (Lead-PI: Xun Jiao)
Year: 2022 - 2025. Total = $385,000; My share = $194,111.

- **As Co-Principal Investigator**

Samsung **Title: Miniaturized Distributed Training of Large Language Models over CXL Devices**
Global Research Outreach (GRO) Program
Role: Co-PI (PI: Yiran Chen; Co-PI: Bryan S. Kim)
Year: 2024 - 2025. My share = $75,000.

SRC **Title: Exploiting Dynamic Sparsity For Training**
GRC 2023 Artificial Intelligence Hardware Program (AIHW)
Role: Co-PI (PI: Nishil Rakeshkumar Talati)
Year: 2024 - 2026. My share = $157,500.

NSF **Title: FuSe-TG: Physical Computing Co-Design using Three-terminal Devices**
Computer and Information Science and Engineering (CISE)
Role: Co-PI (PI: Jennifer Hasler; Co-PIs: Matthew Marinella, Yiyang Li)
Year: 2023 - 2024. My share = $7,500.

NSF **Title: JUMP2.0: CHIMES: Center for Heterogeneous Integration of Micro Electronic Systems**
SRC and DARPA
Role: Co-PI (Center Director: Madhavan Swaminathan, Muhannad Bakir)
Year: 2023 - 2027. My share = $375,000.

NSF **Title: SHF: Medium: Automated End-to-End Synthesis for Programmable Analog & Mixed-Signal Systems**
Computer and Information Science and Engineering (CISE)
Role: Co-PI (PI: Jennifer Hasler)
Year: 2022 - 2026. Total = $1,200,000; My share = $400,000.

DARPA **Title: Ultra-Light Video Intelligence by Data-Circuit-Model Tri-Design: In-Pixel Filtering, In-Memory Focusing, and In-Loop Optimization**
Artificial Intelligence Exploration (AIE)
Role: Co-PI (PI: Shimeng Yu; Co-PIs: Shiyu Chang, Atlas Wang, Sijia Liu)
Year: 2021-2023. Total = $1,000,000; My share = $200,000.

PUBLICATIONS

‡: Student supervised by Dr. Hao
†: Student co-supervised by Dr. Hao
*: Corresponding author

• Book Chapters

[B1] Xiaofan Zhang, Yao Chen, **Cong Hao**, Sitao Huang, Yuhong Li, and Deming Chen, "Compilation and Optimizations for Efficient Machine Learning on Embedded Systems," *In Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing, Springer Nature*, 2023

• Journals

[J1] Afolabi Ige, Linhao Yang, Hang Yang[†], Jennifer Hasler, and **Cong Hao**, "Analog System High-Level Synthesis for Energy-Efficient Reconfigurable Computing", *Journal of Low Power Electronics and Applications*, October 2023

[J2] Jennifer Hasler, **Cong Hao**, "Programmable Analog System Benchmarks leading to Efficient Analog Computation Synthesis", *ACM Transactions on Reconfigurable Technology and Systems*, September 2023

[J3] Nan Wu[†], Yuan Xie, and **Cong Hao***, "IronMan-Pro: Multi-objective Design Space Exploration in HLS via Reinforcement Learning and Graph Neural Network based Modeling", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, June 2022

[J4] **Cong Hao**, Jordan Dotzel, Jinjun Xiong, Luca Benini, Zhiru Zhang, and Deming Chen, "Enabling Design Methodologies and Future Trends forEdge AI: Specialization and Co-design", *IEEE Design & Test*, 2021

[J5] Cheng Gong, Ye Lu, Tao Li, **Cong Hao**, Deming Chen, and Yao Chen, "VecQ: High Accuracy DNN Model Compression with Vectorized Weight Quantization", *IEEE Transactions of Computers*, 2020

[J6] Jianwei Zheng, Chao Lu, **Cong Hao**, Deming Chen, and Donghui Guo, "Improving the Generalization Ability of Deep Neural Networks for Cross-Domain Visual Recognition", *IEEE Transactions on Cognitive and Developmental Systems*, 2020

[J7] Zhao Yi, **Cong Hao**, and Takeshi Yoshimura, "Thermal and Wirelength Optimization With TSV Assignment for 3D-IC", *IEEE Transactions on Electron Devices*, 2019

[J8] Ma Jiayi, **Cong Hao**, and Kundong Wang, "Decomposing and Cluster Refinement Design Method for Application-Specific Network-on-Chips", *Journal of Shanghai Jiao Tong University (Science)*, 2018

[J9] **Cong Hao**, Takeshi Yoshimura, "An Efficient Multi-Level Algorithm for 3D-IC TSV Assignment", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, March 2017

[J10] **Cong Hao**, Nan Wang, and Takeshi Yoshimura, "A Unified Scheduling Approach for Power and Resource Optimization with Multiple V-dd or/and V-th in High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2017.

[J11] **Cong Hao**, Jianmo Ni, Nan Wang, and Takeshi Yoshimura. "Interconnection Allocation between Functional Units and Registers in High-Level Synthesis", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[J12] Wang Nan, Wei Zhong, **Cong Hao**, Song Chen, Takeshi Yoshimura, and Yu Zhu, "Leakage-power-aware scheduling with dual-threshold voltage design", *IEEE Transactions on Very Large Scale Integration Systems*, September 2016.

[J13] Nan Wang, Song Chen, **Cong Hao**, Haoran Zhang, and Takeshi Yoshimura, "Leakage Power Aware Scheduling in High-Level Synthesis", *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, 2014

• Conferences

[C1] Hanqiu Chen[‡], Yitu Wang, Vitorio Cargnini, Mohammadreza Soltaniyeh, Dongyang Li, Gongjin Sun, Pradeep Subedi, Andrew Chang, Yiran Chen and **Cong Hao***, "ICGMM: CXL-enabled Memory Expansion with Intelligent Caching Using Gaussian Mixture Model", IEEE/ACM Design Automation Conference (DAC), 2024

[C2] Stefan Abi-Karam[‡], Rishov Sarkar[‡], Dejia Xu, Zhiwen Fan, Zhangyang Wang, and **Cong Hao***, "INR-Arch: A Dataflow Architecture and Compiler for Arbitrary-Order Gradient Computations in Implicit Neural Representation Processing", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023

[C3] Rishov Sarkar[‡], Hanxue Liang, Zhiwen Fan, Zhangyang Wang, and **Cong Hao***, "Edge-MoE: Memory-Efficient Multi-Task Vision Transformer Architecture with Task-level Sparsity via Mixture-of-Experts" IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023

[C4] Hanqiu Chen[‡], Hang Yang[‡], Stephen BR Fitzmeyer[‡], and **Cong Hao***, "Rapid-INR: Storage Efficient CPU-free DNN Training Using Implicit Neural Representation", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023

[C5] Nan Wu[†], Yingjie Li, **Cong Hao**, Steve Dai, Cunxi Yu, and Yuan Xie, "Gamora: Graph Learning based Symbolic Reasoning for Large-Scale Boolean Networks", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2023, **Best Paper Award**

[C6] Stefan Abi-Karam[‡], and **Cong Hao***, "GNNBuilder: An Automated Framework for Generic Graph Neural Network Accelerator Generation, Simulation, and Optimization", 33rd International Conference on Field-Programmable Logic and Applications (FPL), 2023, **FPL Community Award**

[C7] Rishov Sarkar[‡], and **Cong Hao***, "LightningSim: Fast and Accurate Trace-Based Simulation for High-Level Synthesis", The International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2023, **Best Paper Runner-up**

[C8] Yuhong Li, Jiajie Li, **Cong Hao**, Pan Li, Jinjun Xiong, Deming Chen, "Extensible and Efficient Proxy for Neural Architecture Search", Proceedings of the IEEE/CVF International Conference on Computer Vision (ICCV), 2023

[C9] Hanqiu Chen[‡], and **Cong Hao***, "DGNN-Booster: A Generic FPGA Accelerator Framework For Dynamic Graph Neural Network Inference", short paper, The International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2023

[C10] Lakshmi Sathidevi[‡], Abhinav Sharma[‡], Nan Wu, Xun Jiao, and **Cong Hao***, "PreAxC: Error Distribution Prediction for Approximate Computing Quality Control using Graph Neural Networks", International Symposium on Quality Electronic Design (ISQED), 2023

[C11] Akshay Karkal Kamath[‡], Stefan Abi-Karam[‡], Ashwin Bhat, and **Cong Hao***, "M5: Multi-modal Multi-Task Model Mapping on Multi-FPGA with Accelerator Configuration Search", Design, Automation & Test in Europe Conference & Exhibition (DATE), 2023.

[C12] Rishov Sarkar[‡], Stefan Abi-Karam[‡], Yuqi He[‡], Lakshmi Sathidevi[‡], and **Cong Hao***, "FlowGNN: A Dataflow Architecture for Universal Graph Neural Network Inference via Multi-Queue Streaming", IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2023

[C13] Hanqiu Chen[‡], Yihan Jiang[‡], Yahya AlHinai[‡], Eunjee Na[‡], and **Cong Hao***, "Bottleneck Analysis of Dynamic Graph Neural Network Inference on CPU and GPU", IEEE International Symposium on Workload Characterization (IISWC), 2022

[C14] Haoyu Peter Wang, Nan Wu, Hang Yang[‡], **Cong Hao**, and Pan Li, "Unsupervised Learning for Combinatorial Optimization with Principled Objective Design", Neural Information Processing Systems (NeurIPS), 2022

[C15] Hanxue Liang, Zhiwen Fan, Rishov Sarkar[‡], Ziyu Jiang, Tianlong Chen, Kai Zou, Yu Cheng, **Cong Hao**, and Zhangyang Wang, "M^{3}ViT: Mixture-of-Experts Vision Transformer for Efficient Multi-task Learning with Model-Accelerator Co-design", Neural Information Processing Systems (NeurIPS), 2022

[C16] Yimeng Zhang, Akshay Karkal Kamath[‡], Qiucheng Wu, Zhiwen Fan, Wuyang Chen, Zhangyang Wang, Shiyu Chang, Sijia Liu, and **Cong Hao***, "Data-Model-Circuit Tri-design for Ultra-light Video Intelligence on Edge Devices", IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2022

[C17] Qing Lu, Xiaowei Xu, Shunjie Dong, **Cong Hao**, Lei Yang, Cheng Zhuo, and Yiyu Shi, "RT-DNAS: Real-time Constrained Differentiable Neural Architecture Search for 3D Cardiac Cine MRI Segmentation", International Conference on Medical Image Computing and Computer Assisted Intervention (MICCAI), 2022

[C18] Zishen Wan, Ashwin Lele, Bo Yu, Shaoshan Liu, Yu Wang, Vijay Janapa Reddi, **Cong Hao**, and Arijit Raychowdhury, "Robotic Computing on FPGAs: Current Progress, Research Challenges, and Opportunities", IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2022, **Invited**

[C19] Hanqiu Chen[‡], and **Cong Hao***, "Mask-Net: A Hardware-efficient Object Detection Network with Masked Region Proposals", IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2022

[C20] Nan Wu[†], Jiwon Lee[‡], Yuan Xie, and **Cong Hao***, "LOSTIN: Logic Optimization via Spatio-Temporal Information with Hybrid Graph Models", IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2022, **Best Paper Nomination**

[C21] Nan Wu[†], Hang Yang[‡], Yuan Xie, Pan Li, and **Cong Hao***, "High-Level Synthesis Performance Prediction using GNNs: Benchmarking, Modeling, and Advancing", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2022.

[C22] Xinyi Zhang, **Cong Hao**, Peipei Zhou, Alex Jones, and Jingtong Hu, "H2H: Heterogeneous Model to Heterogeneous System Mapping with Computation and Communication Awareness", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2022.

[C23] Hanchen Ye, **Cong Hao**, Jianyi Cheng, Hyunmin Jeong, Jack Huang, Stephen Neuendorffer, and Deming Chen, "ScaleHLS: A New Scalable High-Level Synthesis Framework on Multi-Level Intermediate Representation", IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2022

[C24] Yuhong Li, **Cong Hao**, Pan Li, Jinjun Xiong, and Deming Chen, "Generic Neural Architecture Search via Regression", International Conference on Neural Information Processing Systems (NeurIPS), 2021, **Spotlight**

[C25] Xinheng Liu, Yao Chen, **Cong Hao**, Ashutosh Dhar, and Deming Chen, "WinoCNN: Kernel Sharing Winograd Systolic Array for Efficient Convolutional Neural Network Acceleration on FPGAs", IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2021

[C26] Yao Chen, Cole Hawkins, Kaiqi Zhang, Zheng Zhang, and **Cong Hao***, "3U-EdgeAI: Ultra-Low Memory Training, Ultra-Low Bitwidth Quantization, and Ultra-Low Latency Acceleration", ACM Great Lakes Symposium on VLSI (GLSVLSI), 2021, **Invited**

[C27] Nan Wu, Yuan Xie, and **Cong Hao***, "IronMan: GNN-assisted Design Space Exploration in High-Level Synthesis via Reinforcement Learning", ACM Great Lakes Symposium on VLSI (GLSVLSI), 2021, **Best Paper Award**

[C28] **Cong Hao**, and Deming Chen, "Software/Hardware Co-design for Multi-modal Multi-task Learning in Autonomous System", IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2021, **Invited**

[C29] Lixiang Li, Yao Chen, Zacharie Zirnheld, Pan Li, and **Cong Hao***, "MeLoPPR: Software/Hardware Co-design for Memory-efficient Low-latency Personalized PageRank", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2021.

[C30] Dongning Ma, Rahul Thapa, Xingjian Wang, **Cong Hao** and Xun Jiao, "Workload-Aware Approximate Computing Configuration", IEEE/ACM Design, Automation & Test in Europe Conference (DATE), 2021.

[C31] Yuhong Li*, **Cong Hao***, Xiaofan Zhang, Chen Yao, Jinjun Xiong, Wen-mei Hwu, and Deming Chen, "EDD: Efficient Differentiable DNN Architecture and Implementation Co-search for Embedded AI Solutions", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2020.

[C32] Xiaofan Zhang, Haoming Lu, **Cong Hao**, Jiachen Li, Bowen Cheng, Yuhong Li, Kyle Rupnow, Jinjun Xiong, Thomas Huang, Honghui Shi, Wen-mei Hwu, and Deming Chen, "SkyNet: a Hardware-Efficient Method for Object Detection and Tracking on Embedded Systems", The Conference on Machine Learning and Systems (SysML), 2020.

[C33] Pengfei Xu, Xiaofan Zhang, **Cong Hao**, Yang Zhao, Zetong Guan, Yongan Zhang, Yue Wang, Deming Chen, and Yingyan Lin, "AutoDNNchip: An Automated DNN Chip Generator through Compilation, Optimization, and Exploration", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2020.

[C34] **Cong Hao**, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, Junli Gu, and Deming Chen, "NAIS: Neural Architecture and Implementation Search and its Applications in Autonomous Driving", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019.

[C35] **Cong Hao**, Xiaofan Zhang, Yuhong Li, Sitao Huang, Jinjun Xiong, Kyle Rupnow, Wen-Mei Hwu, and Deming Chen, "FPGA/DNN Co-Design: An Efficient Design Methodology for IoT Intelligence on the Edge", Proceedings of IEEE/ACM Design Automation Conference (DAC), 2019.

[C36] **Cong Hao**, Atif Sarwari, Bryan Wu, Zhijie Jin, Junli Gu, and Deming Chen, "FPGA-based Secondary System for Autonomous Driving Cars", Proceedings of IEEE International Workshop on Signal Processing Systems, 2019.

[C37] Yao Chen, Kai Zhang, Cheng Gong, **Cong Hao**, Xiaofan Zhang, Tao Li, and Deming Chen, "TDLA: An Open-source Deep Learning Accelerator for Ternarized DNN Models on Embedded FPGA", Proceedings of IEEE Computer Society Annual Symposium on VLSI, 2019.

[C38] Cheng Gong, Ye Lu, **Cong Hao**, Xiaofan Zhang, Tao Li, Deming Chen, and Yao Chen, "μL2Q: An Ultra-Low Loss Quantization Method for DNN Compression", Proceedings of International Joint Conference on Neural Networks (IJCNN), 2019.

[C39] Xiaofan Zhang, **Cong Hao**, Yuhong Li, Yao Chen, Jinjun Xiong, Wen-Mei Hwu, and Deming Chen, "A Bi-Directional Co-Design Approach to Enable Deep Learning on IoT Devices", Joint Workshop on On-Device Machine Learning & Compact Deep Neural Network Representations, ICML Workshop, 2019, **Best Poster Award**

[C40] Yao Chen, Jiong He, Xiaofan Zhang, **Cong Hao**, and Deming Chen, "Cloud-DNN: An Open Framework for Mapping DNN Models to Cloud FPGAs", Proceedings of ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), 2019.

[C41] **Cong Hao**, and Deming Chen, "Deep Neural Network Model and FPGA Accelerator Co-design: Opportunities and Challenges", Proceedings of IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018.

[C42] Sitao Huang, Mohamed El-Hadedy, **Cong Hao**, Qin Li, Vikram S Mailthody, Ketan Date, Jinjun Xiong, Deming Chen, Rakesh Nagi, and Wen-mei Hwu, "Triangle Counting and Truss Decomposition using FPGA", IEEE High Performance extreme Computing Conference (HPEC), 2018

[C43] Yi Zhao, **Cong Hao**, and Takeshi Yoshimura, "TSV Assignment of Thermal and Wirelength Optimization for 3D-IC Routing", In 28th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2018

[C44] **Cong Hao**, and Takeshi Yoshimura, "Application of on-line machine learning in optimization algorithms: A case study for local search", Computer Science and Electronic Engineering (CEEC), IEEE, 2017

[C45] Yangyizhou Wang, **Cong Hao**, and Takeshi Yoshimura, "A Particle Swarm Optimization and Branch and Bound Based Algorithm for Economical Smart Home Scheduling", In 20th IEEE MWSCAS, 2017

[C46] Yuxin Qian, **Cong Hao**, and Takeshi Yoshimura, "3D-IC signal TSV assignment for thermal and wirelength optimization", In 27th IEEE International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2017

[C47] Jiayi Ma, **Cong Hao**, and Takeshi Yoshimura, "Power-efficient Partitioning and Cluster Generation Design for Application-Specific Network-on-Chip", In 13th IEEE ISOCC, 2016

[C48] Hui Zhu, **Cong Hao**, and Takeshi Yoshimura, "Thermal-Aware Floorplanning for NoC-Sprinting", In 59th IEEE MWSCAS, 2016

[C49] **Cong Hao**, and Takeshi Yoshimura, "Economical Smart Home Scheduling for Single and Multiple Users", In 59th IEEE MWSCAS, 2016

[C50] **Cong Hao**, Nan Ding, and Takeshi Yoshimura, "An Efficient Algorithm for 3D-IC TSV Assignment", In 14th IEEE NEWCAS, 2016, **Best Student Paper**

[C51] **Cong Hao**, Takeshi Yoshimura, "EACH: An Energy-Efficient High-Level Synthesis Framework for Approximate Computing", In 2nd IEEE WAPCO, 2016

[C52] Jian-Mo Ni, Qian Ai, **Cong Hao**, Takeshi Yoshimura, and Nan Wang, "Primal-Dual Method based Simultaneous Functional Unit and Register Binding", In 10th ASICON, 2015

[C53] **Cong Hao**, Nan Wang, Jian-Mo Ni, and Takeshi Yoshimura, "An Efficient Tabu Search Methodology for Port Assignment Problem in High-Level Synthesis", In 24th IWLS, 2015

[C54] **Cong Hao**, Jian-Mo Ni, Hui-Tong Wang, and Takeshi Yoshimura, "Simultaneous Scheduling and Binding For Resource Usage and Interconnect Complexity Reduction in High-Level Synthesis", In 11th IEEE ASICON, 2015, **Best Student Paper**

[C55] **Cong Hao**, Song Chen, and Takeshi Yoshimura, "Network simplex method based Multiple Voltage Scheduling in Power-efficient High-level synthesis", In 18th IEEE ASP-DAC, 2013, **IEICE VLD Excellent Student Award**

[C56] **Cong Hao**, Nan Wang, Song Chen, Takeshi Yoshimura, and Min-You Wu, "Interconnection allocation between functional units and registers in High-Level Synthesis", In 10th IEEE ASICON, 2013, **Best Student Paper**

[C57] Wang Nan, **Cong Hao**, Nan Liu, Haoran Zhang, and Takeshi Yoshimura, "Timing and resource constrained leakage power aware scheduling in high-level synthesis", In 10th IEEE ASICON, 2013

[C58] **Cong Hao**, Haoran Zhang, Song Chen, Takeshi Yoshimura, and Min-You Wu, "Port assignment for multiplexer and interconnection optimization", In 5th IEEE ASQED, 2013

[C59] Haoran Zhang, **Cong Hao**, Nan Wang, Song Chen, and Takeshi Yoshimura, "Power and resource aware scheduling with multiple voltages", In 10th IEEE ASICON, 2013, **Best Student Paper**

[C60] **Cong Hao**, Song Chen, and Takeshi Yoshimura, "Port assignment for interconnect reduction in high-level synthesis", In 19th IEEE VLSI-DAT, 2012, **Best Paper Nomination**

KEYNOTE AND INVITED TALKS

Feb. 2024 "Ultra-Low-Latency Graph Neural Networks: Applications and Implementations"
HPCS Lab, UNC-Charlotte (virtual)

Dec. 2023 **Keynote** "Ultra-Low-Latency Graph Neural Networks: Applications and Implementations"
The 7th Workshop on Graph Techniques for Adversarial Activity Analytics (GTA^3 2023), Sorrento, Italy (hybrid)

Jul. 2023 "Smart Reconfigurable Computing for GNNs and Transformers + Smart HLS tool"
4th ROAD4NN workshop @ DAC'23, San Francisco

Mar. 2023 "Multi-task Vision Transformer with Mixture-of-Expert: Algorithm and Accelerator"
The Conference on Information Sciences and Systems (CISS), Baltimore, MD

Feb. 2023 "Smart Reconfigurable Computing for GNNs and Transformers"
University of California, Santa Barbara, CA

Feb. 2023 "Smart Reconfigurable Computing for GNNs and Transformers"
ECE Distinguished Speaker Colloquium, North Carolina State University, NC

Feb. 2023 "Multi-task Vision Transformer with Mixture-of-Expert: Algorithm and Accelerator"
Georgia Tech CRNCH Summit, Atlanta, GA

Dec. 2022 "Generic and Automated Graph Neural Network Acceleration"
UIUC HACC Monthly Seminar, Virtual

Dec. 2022 "Generic and Automated Graph Neural Network Acceleration"
hls4ml Monthly Seminar, Virtual

Dec. 2022 "Generic and Automated Graph Neural Network Accelerator"
FAI Summit, 2022, Virtual

Nov. 2022 "The DAC System Design Contest 2018 – 2022: Lessons Learned in Edge Computing"
4th Workshop on Accelerator Computer Aided Design (ACCAD), Virtual

Oct. 2022 "Tutorial: Embedded Machine Learning: Design, Optimizations, and Applications"
ESWEEK 2022, Tutorial, Virtual

Jul. 2022 "Tutorial: A Journey to SW/HW Co-design in Machine Learning: Fundamental, Advancement, and Application"
IEEE/ACM DAC 2022, Tutorial, San Francisco

Jul. 2022 "3U-EdgeAI: Ultra-Low Memory Training, Ultra-Low Bitwidth Quantization, and Ultra-Low Latency Acceleration"
IEEE/ACM DAC 2022, DACPS Workshop, San Francisco

May 2022 "H2H: Heterogeneous Model to Heterogeneous System Mapping"
Tenstorrent Inc., virtual

Apr. 2022 "Deep Neural Network and Accelerator Co-design: Present and Future"
Salishan Conference on High Speed Computing, virtual

Feb. 2022 "Deep neural network and accelerator co-design"
SIAM Conference on Parallel Processing for Scientific Computing (PP22) Minisymposium, virtual

Feb. 2022 "GenGNN: a Generic FPGA Acceleration Framework for Graph Neural Networks"
Georgia Tech CRNCH Summit, virtual

Oct. 2021 "How Powerful are Graph Neural Networks and Reinforcement Learning in EDA: a Case Study in High-Level Synthesis"
Stevens Institute of Technology ECE Seminar, virtual

Sep. 2021 "How Powerful are Graph Neural Networks and Reinforcement Learning in EDA: a Case Study in High-Level Synthesis"
Rutgers EFficient AI (REFAI) Seminar, virtual

Jun. 2021 "Software/Hardware Co-Design for Multimodal Multi-Task Learning in Autonomous Systems"
IEEE AICAS 2021, special session, virtual

Jun. 2021 "3U-EdgeAI: Ultra-Low Memory Training, Ultra-Low Bit-width Quantization, and Ultra-Low Latency Acceleration"
ACM GLSVLSI 2021, special session, virtual

Nov. 2019 "NAIS: neural architecture and implementation co-search"
IEEE/ACM ICCAD 2019, special session, Denver, CO

TEACHING EXPERIENCE

Fall 2023 Georgia Tech, ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)
Graduate-level class of 83 students, CIOS score: 4.4/5.0

Spring 2023 Georgia Tech, ECE8893 (Parallel Programming for FPGAs)
Graduate-level class of 44 students, CIOS score: 4.8/5.0

Fall 2022 Georgia Tech, ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)
Graduate-level class of 82 students, CIOS score: 4.6/5.0

Spring 2022	Georgia Tech, ECE8893 (Parallel Programming for FPGAs) Graduate-level class of 38 students, CIOS score: 4.7/5.0
Fall 2021	Georgia Tech, ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture) Graduate-level class of 68 students, CIOS score: 4.2/5.0
Fall 2019	University of Illinois at Urbana-Champain, ECE 498 (IoT and Cognitive Computing) Guest Lecturer
Spring 2018	University of Illinois at Urbana-Champain, ECE 527 (System-on-Chip Design) Guest Lecturer

Student Advising

• PhD Students (In Progress)

- **Rishov Sarkar**, 2021 Fall – present
- **Hanqiu Chen**, 2022 Fall – present
- **Hang Yang**, 2022 Fall – present
- **Stefan Abi-Karam**, 2023 Spring – present
- **Lakshmi Sathidevi**, 2023 Fall – present
- **Jiho Kim**, 2023 Fall – present

• MS Students (Graduated)

- **Stefan Abi-Karam**, 2021 Fall – 2022 Fall, GaTech Ph.D.
  Thesis: GNNBuilder: an Automated Framework for Generic Graph Neural Network Accelerator Generation, Simulation, and Optimization
- **Akshay Karkal Kamath**, 2021 Fall – 2023 Spring, Apple Inc.
  Thesis: Scalable Hardware Accelerator Design for State-of-the-art Computer Vision Algorithms

Professional Services

• Associate Editor

2020-present	Neural Processing Letters (Springer)

• Conference and Workshop Organization

2024	Finance Chair of LAD'24 (first IEEE International Workshop on LLM-Aided Design)
2024	Program Vice Chair of FCCM'24
2023	Publicity chair of FCCM'23
2022	ICCAD'22 TPC chair, DATE'22 TPC Co-chair
2022	Organizer of DAC'22 Early Career Workshop
2022	Chair of ACM Student Research Competition at ICCAD (SRC@ICCAD22)
2022	Organizer of DAC'22 Software/Hardware Co-design Tutorial
2021	Publicity chair of FCCM'22
2021	Co-organizer of ICCV'21 Workshop (low-power computer vision)
2021	Co-chair of 58th IEEE/ACM Design Automation Conference System Design Competition (DAC-SDC) at DAC'21
2021	Co-chair of ACM Student Research Competition at ICCAD (SRC@ICCAD21)

• Technical Program Committee

2024 FPGA'24, DAC'24
2023 FPGA'23, FCCM'23, ICCAD'23
2022 TinyML'22, FCCM'22, DAC'22, ICCAD'22, DATE'22
2021 DAC'21, DATE'21, ICCD'21, ICCV'21 (workshop)
2020 DATE'20, ICCD'20, SRC@ICCAD'20, CENICS'20
2019 CENICS'19

• Session Chair

2023 DAC'23
2022 DAC'22, ICCAD'22
2022 ISQED'22
2021 ICCV'21 Workshop, GLSVLSI'21
2020 ICCD'20, DATE'20

• Journal Review

IEEE Journal on Selected Areas in Communications
Engineering Optimization
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI)
IEEE Design & Test (D&T)
Multidimensional Systems & Signal Process (MULT)
ACM Transactions on Design Automation of Electronic Systems (TODAES)
IEEE Internet of Things Journal
ACM Journal on Emerging Technologies in Computing Systems (JETC)
IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
ACM Transactions on Embedded Computing Systems (TECS)
IEEE Transactions on Computers (TC)
ACM Transactions on Architecture and Code Optimization (TACO)
IEEE Sensors Letters
IEEE Transactions on Circuits and Systems I (TCAS-I)
IEEE Transactions on Sustainable Computing (T-SUSC)

• Panel Review

2022 – 2024 National Science Foundation (NSF)
2024 Army Research Office (ARO)
2023 Natural Sciences and Engineering Research Council of Canada (NSERC)
2023 Nazarbayev University (Kazakhstan)
2022 Research Grants Council Hong Kong (2022)